AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 4, line 27, with the following amended paragraph:

~~FIG. 5~~FIGS. 5A - C depict~~s~~ the sixth method step--insulating the ends of the upwardly penetrating metal layer;

Please replace the paragraph beginning on page 6, line 6, with the following amended paragraph:

The insulating layer 3 also covers the side surfaces of the semiconductor columns 1. A first conductive metal layer 4, which later on constitutes the gate electrode of the transistor, is deposited on the insulating layer 3 by sputtering, vaporization, chemical vapor deposition or a similar process. Thereafter, a further insulating layer 5 is deposited (FIG. 3), and the upper layer of the laminate formed in this manner is etched planar (FIG. 4). This may be done by a horizontal ion beam (ion beam etching) or by plasma, chemical or electrochemical etching processes of the kind sufficiently known in semiconductor technology. Thereafter, the upwardly penetrating ends of the metal layer 4 are insulated ~~(FIG. 5)~~. This may be carried out by etching back the metal protruding to the surface by a metal-specific etching step (FIG. 5A) and by applying a further insulating layer 10 (FIG. 5B) which is planarized in turn (FIG. 5C). Alternatively, as shown in FIG. 5C, the metal protruding to the surface may be converted to an insulator 6 by chemical oxidizing or nitriding. Finally, a second metal layer 7 is deposited (FIG. 6). This metal layer is electrically connected to the semiconductor column, and later on it serves as source electrode and drain electrode.